CLAIMS

What is claimed is:

1. A method comprising:

issuing a cache residency test instruction for a set of data; and

determining with a processor unit using the issued cache residency test instruction if the set of data resides in a cache memory that is communicatively coupled to the processor unit; and

communicating a result of the determining to software being executed on the processor unit.

2. A method as described in claim 1, wherein the determining further comprises:

querying whether the set of data resides in the cache memory; and

receiving an indication at the processor unit from the querying which indicates whether the set of data resides in the cache memory.

3. A method as described in claim 1, wherein the software is selected from the group consisting of an operating system and an application.

4. A method as described in claim 1, further comprising, after the determining, establishing a relative amount of time to access the set of data by the processor unit.

5. A method as described in claim 1, wherein the set of data is selected from the group consisting of:

an instruction for controlling the processor unit; and

data for being processed by the processor unit.

6. A method as described in claim 1, wherein the cache memory is selected from the group consisting of:

a cache memory for storing an instruction for controlling the processor unit;

a cache memory for storing data for being processed by the processor unit; and

a combination of the forgoing.

7. A method as described in claim 1, wherein the determining is performed without reading the set of data into the processor unit from the cache memory unit and without writing the set of data from the processor unit into the cache memory.

8. A method as described in claim 1, further comprising:

comparing an address of the set data with at least one other address in the cache memory, wherein the cache memory includes a plurality of levels; and

indicating, based on the comparing, to the processor unit whether the address of the set of data is included in the cache memory, wherein if the address is included in the cache memory, the indicating indicates at which level of the plurality of levels the address is included.

9. A method as described in claim 1, wherein the cache memory is configured as a semiconductor-based memory.

10. One or more computer-readable media comprising computer-executable instructions that, when executed, perform the method as recited in claim 1.

11. A method comprising:

querying whether a set of data resides in a cache memory that is communicatively coupled to a processor unit;

receiving an indication at the processor unit from the querying which indicates whether the set of data resides in the cache memory; and

communicating the indication to software being executed on the processor unit.

12. A method as described in claim 11, wherein the software is selected from the group consisting of an operating system and an application.

13. A method as described in claim 11, further comprising establishing a relative amount of time to access the set of data by the processor unit based on the indication which indicates whether the set of data resides in the cache memory.

14. A method as described in claim 11, wherein the set of data is selected from the group consisting of:

an instruction for controlling the processor unit; and

data for being processed by the processor unit.

15. A method as described in claim 11, wherein the cache memory is selected from the group consisting of:

a cache memory for storing an instruction for controlling the processor unit;

a cache memory for storing data for being processed by the processor unit; and

a combination of the forgoing.

16. A method as described in claim 11, wherein the querying and the receiving are performed without reading the set of data from the cache memory to the processor unit and without writing the set of data from the processor unit to the cache memory.

17. A method as described in claim 11, further comprising:

comparing an address of the set data with at least one other address in the cache memory, wherein the cache memory includes a plurality of levels; and

providing, based on the comparing, an indication to the processor unit of whether the address of the set of data is included in the cache memory, wherein if the address is included in the cache memory, the indication indicates at which level of the plurality of levels the address is included.

18. One or more computer-readable media comprising computer-executable instructions that, when executed, perform the method as recited in claim 11.

19. A method comprising:

comparing an address of a set data with at least one other address in a cache memory, wherein the cache memory includes a plurality of levels and is communicatively coupled to a processor unit;

providing an indication to the processor unit, based on the comparing whether the address of the set of data is included in the cache memory, wherein if the address is included in the cache memory, the indication indicates at which level of the plurality of levels the address is included; and

communicating the indication, by the processor unit, to software being executed on the processor unit.

20. A method as described in claim 19, further comprising establishing a relative amount of time to access the set of data, by the processor unit, based on which level of the plurality of levels the address is included.

21. A method as described in claim 19, wherein the software is selected from the group consisting of an operating system and an application.

22. A method as described in claim 19, wherein the cache memory is selected from the group consisting of:

a cache memory for storing an instruction for controlling the processor unit;

a cache memory for storing data for being processed by the processor unit; and

a combination of the forgoing.

23. One or more computer-readable media comprising computer-executable instructions that, when executed, perform the method as recited in claim 19.

24. A method comprising:

supplying an address for a set of data to a comparison unit from a processor unit;

comparing with the comparison unit the address for the set of data with an address in the cache memory;

indicating to the processor unit from the comparison unit based on the comparing whether the address of the set of data is included in the cache memory;

establishing based on the indicating of whether the address of the set of data is included in the cache memory a relative amount of time to access the set of data by the processor unit; and

communicating the established relative amount of time to software being executed by the processor unit.

25. A method as described in claim 24, wherein the access to the set of data by the processor unit is selected from the group consisting of:

writing the set of data; and

reading the set of data.

26. A method as described in claim 24, wherein the comparison unit is selected from the group consisting of:

a memory management unit;

a load/store unit; and

a cache controller.

27. A method as described in claim 24, further comprising translating the address of the set of data such that a format of the address of the set of data corresponds with a format of the at least one other address in the cache memory.

28. A method as described in claim 24, wherein the cache memory includes a plurality of levels, and the indicating indicates at which level of the plurality of levels the address is included.

29. A method as described in claim 24, wherein the set of data is selected from the group consisting of:

an instruction for controlling the processor unit; and

data for being processed by the processor unit.

30. A method as described in claim 24, wherein the cache memory is selected from the group consisting of:

a cache memory for storing an instruction for controlling the processor unit;

a cache memory for storing data for being processed by the processor unit; and

a combination of the forgoing.

31. A method as described in claim 24, wherein the indicating is performed without reading the set of data from the cache memory to the processor unit and without

writing the set of data from the processor unit to the cache memory.

32. A method as described in claim 24, further comprising signaling that the set of data is to be retained in the cache memory based on the comparison.

33. A method as described in claim 24, wherein the cache memory includes a plurality of levels having addresses of sets of data stored in the levels, and wherein the comparing further comprises comparing the address of the set data with the addresses in the plurality of levels.

34. One or more computer-readable media comprising computer-executable instructions that, when executed, perform the method as recited in claim 24.

35. For use on a processor unit that is communicatively coupled to a cache memory, a cache residency test instruction, executable on the processor unit, which when executed on the processor unit configures the processor unit to performs acts comprising:

querying whether a set of data resides in the cache memory;

receiving an indication from the querying of whether the set of data resides in the cache memory; and

communicating the indication to software being executed on the processor unit.

36. A cache residency test instruction as described in claim 35, wherein the processor unit is communicatively coupled to a comparison unit, and execution of the

cache residency test instruction by the processor unit configures the comparison unit to perform acts including comparing an address of the set of data with at least one other address in the cache memory in response to the querying.

37. A cache residency test instruction as described in claim 35, further comprising establishing a relative amount of time to access the set of data by the processor unit, wherein the establishing is based on the indication which indicates whether the set of data resides in the cache memory.

38. A cache residency test instruction as described in claim 35, wherein the set of data is selected from the group consisting of:

an instruction for controlling the processor unit; and

data for being processed by the processor unit.

39. A cache residency test instruction as described in claim 35, wherein the cache memory is selected from the group consisting of:

a cache memory for storing an instruction for controlling the processor unit;

a cache memory for storing data for being processed by the processor unit; and

a combination of the forgoing.

40. A cache residency test instruction as described in claim 35, wherein the querying and the receiving are performed without reading the set of data from the cache memory to the processor unit and without writing the set of data from the processor unit

to the cache memory.

41. A cache residency test instruction as described in claim 35, wherein the processor unit is communicatively coupled to a comparison unit, and execution of the cache residency test instruction by the processor unit configures the comparison unit to perform acts including:

comparing an address, received from the processor unit from the querying, of the set data with at least one other address in the cache memory, wherein the cache memory includes a plurality of levels; and

providing an indication, based on the comparing, to the processor unit of whether the address of the set of data is included in the cache memory, wherein if the address is included in the cache memory, the indicating indicates at which level of the plurality of levels the address is included.

42. For use on a processor unit that is communicatively coupled to a comparison unit that is communicatively coupled to a cache memory, a cache residency test instruction, which when executed on the processor unit, configures the comparison unit to perform acts comprising:

comparing an address received from the processor unit with an address in the cache memory;

providing an indication to the processor unit based on the comparing of whether the address is included in the cache memory; and

communicating the indication to software being executed by the processor unit.

43. A cache residency test instruction as described in claim 42, wherein the indication indicates to the processor unit whether the address is included in the cache memory, and if so, at which level of a plurality of levels of the cache memory the address is included.

44. A cache residency test instruction as described in claim 42, wherein the cache memory is selected from the group consisting of:

a cache memory for storing an instruction for controlling the processor unit;

a cache memory for storing data for being processed by the processor unit; and

a combination of the forgoing.

45. A system comprising:

a cache memory; and

a processor unit communicatively coupled to the cache memory, wherein the processor unit includes a cache residency test instruction that, when executed, configures the processor unit:

to query whether a set of data resides in the cache memory;

to receive an indication from the query of whether the set of data resides in the cache memory; and

to communicate the indication to software being executed on the processor unit.

46. A system as described in claim 45, further comprising a comparison unit, wherein execution of the cache residency test instruction by the processor unit configures the comparison unit to compare an address of the set of data with at least one other address of the cache memory in response to the query.

47. A system as described in claim 45, wherein the processor unit establishes a relative amount of time to access the set of data by the processor unit based on the indication.

48. A system as described in claim 45, wherein the set of data is selected from the group consisting of:

an instruction for controlling the processor unit; and

data for being processed by the processor unit.

49. A system as described in claim 45, wherein the cache memory is selected from the group consisting of:

a cache memory for storing an instruction for controlling the processor unit;

a cache memory for storing data for being processed by the processor unit; and

a combination of the forgoing.

50. A system as described in claim 45, wherein the cache memory includes a plurality of levels, if the address is included in the cache memory, the indication indicates at which level of the plurality of levels the address is included.

51. A system comprising:

a processor unit;

a comparison unit communicatively coupled to the processor unit; and

a cache memory communicatively coupled to the comparison unit, wherein the comparison unit is configured:

to compare an address received from the processor unit with at least one address in the cache memory; and

to provide an indication to the processor unit indicating whether the address is included in the cache memory based on the comparison.

52. A system as described in claim 51, wherein the comparison unit is selected from the group consisting of:

a memory management unit (MMU);

a load/store unit; and

a cache controller.

53. A system as described in claim 51, wherein the set of data is selected from the group consisting of:

an instruction for controlling the processor unit; and

data for being processed by the processor unit.

54. A system as described in claim 51, wherein the cache memory is selected

from the group consisting of:

a cache memory for storing an instruction for controlling the processor unit;

a cache memory for storing data for being processed by the processor unit; and

a combination of the forgoing.

55. A system as described in claim 51, wherein the cache memory includes a plurality of cache memory levels, the comparison unit is configured to provide an indication which indicates if the address of the set of data is included in the cache memory, at which level of the plurality of levels the address of the set of data is included.

56. A processor chip comprising

a processor unit having a coupling for communicatively coupling the processor unit to a cache memory, wherein:

the processor unit includes storage for a cache residency test instruction; and

an execution of the cache residency test instruction with the processor unit configures the processor unit to determine if a set of data resides in the cache memory and communicate a result of the determination to software being executed on the processor unit.

57. A processor chip as described in claim 56, further comprising a second processor unit having:

a coupling for communicatively coupled the second processor unit to the

cache memory;

storage for a second cache residency test instruction; and

an execution of the second cache residency test instruction with the second processor unit configures the second processor unit to determine if a set of data resides in the cache memory and communicate a result of the determination to software being executed on the second processor unit.

58. A processor chip as described in claim 56, wherein the set of data is selected from the group consisting of:

an instruction for controlling the processor unit; and

data for being processed by the processor unit.

59. A processor chip as described in claim 56, wherein the cache memory is selected from the group consisting of:

a cache memory for storing an instruction for controlling the processor unit;

a cache memory for storing data for being processed by the processor unit; and

a combination of the forgoing.

60. A processor chip as described in claim 56, wherein the cache memory is selected from the group consisting of:

a cache memory located on the processor chip;

a cache memory located off the processor chip; and

a combination of the forgoing.

61. A processor chip as described in claim 56, wherein the cache memory is configured as a semiconductor-based memory.

62. A processor chip as described in claim 56, wherein the software is selected from the group consisting of an operating system and an application.

63. A computing device comprising:

a storage device; and

a processor chip, communicatively coupled to the storage device, and including:

a cache memory; and

a processor unit communicatively coupled to the cache memory, wherein the processor unit includes storage for a cache residency test instruction that, when executed by the processor unit, configures the processor unit to determine if a set of data resides in the cache memory and to communicate a result of the determination to software being executed on the processor chip.

64. A computing device as described in claim 63, wherein the processor chip further comprises a second processor unit communicatively coupled to the cache memory, wherein the second processor unit includes storage for a second cache residency test instruction that, when executed by the second processor unit, configures the second processor unit to determine if a set of data resides in the cache memory and to communicate a result of the determination to software being executed on the processor

chip

65. A computing device as described in claim 63, wherein the set of data is selected from the group consisting of:

an instruction for controlling the processor unit; and

data for being processed by the processor unit.

66. A computing device as described in claim 63, wherein the cache memory is selected from the group consisting of:

a cache memory for storing an instruction for controlling the processor unit;

a cache memory for storing data for being processed by the processor unit; and

a combination of the forgoing.

67. A computing device as described in claim 63, wherein the cache memory is configured as a semiconductor-based memory.

68. A computing device as described in claim 63, wherein the software is selected from the group consisting of an operating system and an application.